B' Cont'd

the corresponding plane portion of the junction, since the electric field in the edge region is much higher. The ratio between the breakdown voltage of the edge and the plane portion is thus below unity.

Please rewrite the paragraph beginning on page 5, line 13 to read as follows:

B2

As an alternative, instead of performing, into each of the epitaxial layers 2 and 3 a single implant, several implants can be performed in succession into each of the epitaxial layers 2 and 3. Each implant of the succession is performed with a respective energy, so as to locate the peak dopant concentration at a respective depth. The dose of these implants ranges from 5×10^{12} to 5×10^{13} atoms/cm^2, and the energies range from 100 keV to 900 keV or more. For example, where the implanted dopant is boron, three implants at 300 keV, 600 keV and 900 keV can be performed, so as to have peak dopant concentrations located at a depth of 0.7 μm, 1.2 μm and 1.7 μm, respectively.

Please rewrite the paragraph beginning on page 7, line 14 to read as follows:

B3

It is evident that the number of N type semiconductor layers can be different from six and so can that of the P doped regions inside them, depending on the overall thickness of the drain layer of the final device, i.e., on the voltage to be sustained by the power device.

IN THE CLAIMS

Please amend claims 13, 15, 16, 19-20 to read as follows:

B4

13. (Amended) An integrated edge structure for a high voltage semiconductor device, comprising a number of superimposed semiconductor layers of a first conductivity type and at least two columns of doped regions of a second conductivity type, said columns disposed in said number of superimposed semiconductor layers, wherein, for each column of the at least two columns, the column is deeper than each column of the at least two columns that is farther from said high voltage semiconductor device than the column.

B5

15. (Amended) The integrated edge structure according to claim 13, wherein said number of superimposed semiconductor layers is superimposed on a semiconductor substrate.